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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,972	09/26/2003	Masakatsu Uneme	N28733102E	3617

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,972	UNEME, MASAKATSU	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on November 13, 2006 regarding application 10,672,972 filed on September 26, 2003.

2. Claims 1-2, 7-8, 11-15 and 20 have been amended.

Claims 1-21 are pending in the application under consideration.

3. ***Response to Amendments and Remarks***

Applicant's remarks have been fully and carefully considered with the Examiner's response set forth below.

Applicants amended claims 1-2, 7-8, 11-15 and 20 with additional limitations. Some of the added limitations raise issues under 35 USC § 112. Refer to the following claim analysis for details. As such, claims 1-14 will not be further analyzed in this Office Action to assess their merits of patentability, pending on Applicant's clarification.

Another iteration of claim analysis of claims 15-21 based on the same ground via Applicant's admission of prior art (Uneme, US Patent Application Publication 2004/0076002 A1) is presented. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1, as currently amended, recites the limitation of "a circuit core region in which the clock generating circuit and **data generating circuit** are formed; and ..." However, the written description of Applicant's disclosure (Uneme, US Patent Application Publication 2004/0076002) states that "a **data storing circuit**, a clock generating circuit, and an output delay circuit can be formed within the circuit core region" (paragraph [0009]). In other words, the Specification is silent about the existence of **data generating circuit** in the core region. Hence this newly added limitation lacks the support from the written description.

Claims 2-14 are rejected by virtue of their dependency from claim 1.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

First, claim 1 recites the limitation of "each m output holding circuit is adjacent to a corresponding one of the m data output terminals in a first direction between the corresponding data output terminal and the circuit core region; and ..."

The claim language indicates a m-to-one mapping between the holding circuit and the output terminal as it states "each m output holding circuit" is adjacent to "a corresponding one of the m data output terminals." On the other hand, figure 2 of Applicant's disclosure shows a one-to-one correspondence between the two groups. It is not clear what is the intended mapping.

Second, claim 1 also recites the limitation of "an output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) in a first direction between the corresponding data output terminal and the circuit core region."

The claim language indicates that it is "an output" of each output delay circuit that is adjacent to the corresponding p signal output terminal(s), which raises the question whether that "each output delay circuit" itself is adjacent to the p signal output terminal(s), or only "an output" of the output delay circuit is adjacent to the p signal output terminal(s).

Third, the limitation of "a first direction between the corresponding data output terminal and the circuit core region" is indefinite. It is well known that two different points A and B may define one of two possible directions, either from A to B or from B to A. However, it is not clear how a direction may be defined between a point (the corresponding data output terminal) and a region (the circuit core region).

Claims 2-14 are rejected by virtue of their dependency from claim 1.

Claims 1-14 will not be further analyzed in this Office Action to assess their merits of patentability, pending on Applicant's clarification.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 15-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admission of prior art (Uneme, US Patent Application Publication 2004/0076002 A1).

As to claim 15, Applicant's admission of prior art teaches a memory controller connected to a semiconductor memory [figures 10-12; paragraphs 0002-0023], comprising :

a predetermined number 'm" data input terminals that receive input data from the semiconductor memory device [figures 10-12; paragraphs 0002-0023];

a predetermined number "n" signal input terminal, each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data, where m>n [figures 10-12; paragraphs 0013-0014 and 0020-0023];

a data storing circuit for receiving digital data from the data input terminals [figure 11];

n input delay circuits that delay received device input clock signals form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 11, 219; paragraphs 0009-0014 and 0021];

m input holding circuits that hold the input data in synchronism with the input strobe signal generated by the input delay circuit [figure 11]; **and**

m data input wirings, each data input wiring transmitting an input data value from one data input terminal to a corresponding input holding circuit [it is inherent that wirings be present to connect between corresponding points to transmit signal since the Application is not directed toward wireless invention; figure 11 shows the wiring]; **and**

m signal input wirings transforming one input strobe signal from one input delay circuit to a corresponding input holding circuit [it is inherent that wirings be present to connect between corresponding points to transmit signal since the Application is not directed toward wireless invention; figure 11 shows the wiring];

wherein the data input wiring and signal input wiring for the same corresponding input holding circuit being equal in length [[it is assumed that the plurality of wirings 225 distributed between the final stage FFs 218 and data I/O terminals 215 can have the same length (paragraph 0017)].

As to claim 16, Applicant's admission of prior art teaches that **the input delay circuits are arranged between the signal input terminals and locations where the input delay circuits output the input strobe signals** [figure 11, 219].

As to claim 17, Applicant's admission of prior art teaches that **the memory controller of claim 15, wherein: the input holding circuits transmit input data to the data generating circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal** [In DDR-SDRAM, digital data can be input to, or output from the DDR-SDRAM on both the rise and fall of a clock signal (paragraph 0003)].

As to claim 18, Applicant's admission of prior art teaches that **the memory controller of claim 15, further including: the semiconductor memory device being coupled to the memory controller by the m data input terminals and the n signal input terminals** [figure 11].

As to claim 19, Applicant's admission of prior art teaches that **the memory controller of claim 15, further including**:

a circuit core region in which the data storing circuit are formed [paragraph 0009; figure 10]; **and an interface region surrounding the circuit core region in which the data input terminals, input holding circuits, signal input terminals, input delay circuits, signal input wirings, and data input wirings are formed; wherein each input holding circuit comprising a first latch circuit** [figure 10; paragraph 0009].

As to claim 20, Applicant's admission of prior art teaches that **the memory controller of claim 15, further including**:

the m data input terminals and n signal input terminals are aligned with one another in a first direction [figures 10-11]; **and**

the m input holding circuits are aligned with one another in the first direction parallel to the data input terminals and signal input terminals [figures 10-11].

As to claim 21, Applicant's admission of prior art teaches that **the memory controller of claim 15, further including**:

a clock generating circuit that generates an output clock signal [figure 10; paragraph 0011, 0021];

a data generating circuit that provides output digital data [figure 10; paragraph 0012, 0021];

a plurality of data output terminals that that provide output data to the semiconductor memory device in parallel [figure 10; paragraph 0009, 0021];

a signal output terminal for every "q" data output terminals, where "q" is an integer greater than 2, each signal output terminal providing an output strobe signal to the semiconductor memory device in synchronism with the output data [figure 10; paragraphs 0009-0012, 0021];

an output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s) [figure 11; paragraphs 0009-0012, 0021]; **and**

an output holding circuit corresponding to each data output terminal, each group of q output holding circuits holding output data in synchronism with the output strobe signal from the corresponding output delay circuit [figures 10-11; paragraphs 0009-0012, 0021].

9. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Yanagawa, (US Patent Application Publication 2001/0046163), "Memory System and memory Controller with Reliable Data Latch operation."

- Nelson et al., (US 5,258,660), "Skew-Compensated Clock Distribution System."
- Zumkehr, (US Patent Application Publication 2003/0005346), "System and Method for Delaying a Strobe Signal."
- Noda et al., (US Patent Application Publication 2001/0015666), "Semiconductor Integrated Circuit Device, Semiconductor memory System and Clock Synchronous Circuit."

Conclusion

10. Claims 1-21 are rejected as explained above.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

January 3, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
1/4/07